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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/784,087	02/16/2001	Soon-Sung Yoo	8733.405.00	3235
30827	7590	04/08/2004	EXAMINER	
MCKENNA LONG & ALDRIDGE LLP 1900 K STREET, NW WASHINGTON, DC 20006			QI, ZHI QIANG	
			ART UNIT	PAPER NUMBER
			2871	
DATE MAILED: 04/08/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/784,087	YOO ET AL.
Examiner	Art Unit	
Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 12 January 2004 and 09 March 2004.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-5,21 and 22 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 3-5,21 and 22 is/are allowed.

6) Claim(s) 1 and 2 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ .
5) Notice of Informal Patent Application (PTO-152)
6) Other: ____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 9, 2004 has been entered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,825,449 (Shin).

Claim 1, Shin discloses (col.1, line 12 – col.2, line 28; Fig.1 and Fig.6) that a liquid crystal display device comprising:

- substrate (1);
- thin film transistor (TFT) including a gate electrode (2), a source electrode (7), and a drain electrode (8) on the substrate (1);
- pixel electrode (6) electrically connected to the drain electrode (8);

- data line (610) electrically connected with the source electrode (7);
- a gate insulating layer (3) (as a first insulating layer), a pure amorphous silicon layer (4), and a doped amorphous silicon layer (5) sequentially layered under the data line (610) (the date line is connected with the source electrode 7);
- data pad (2A) at one end of the data line (610) (the pad is for communicate information from an external driving circuit to the gate or source electrodes, so that the pad must be at one end of the data line or gate line);
- gate line (600) electrically connected with the gate electrode (26);
- gate pad electrode (6B) at one end of the gate line (600) (the ITO patterns 6A and 6B are formed on the source pad 2A and the gate pad 2B, such that the ITO patterns 6A and 6B must be the pad electrodes);
- the gate pad electrode (6B) is formed of a same material (ITO) and in a same layer (see Fig.1f) as the pixel electrode (6) in a single layer over the gate insulating layer (3) (first insulating layer); and the gate insulating layer (3) includes an opening (see contact hole in Fig.1f) that exposes a portion of the gate line (600), and the gate pad electrode (6B) electrically contacts the exposed portion of the gate line (600) (see Fig.1f, the gate line is connected with the gate pad, and the gate pad electrode connected with the gate pad, so that the gate pad electrode must also contact a portion of the gate line, and the contact hole must expose a portion of the gate line);

- a transparent conductive layer (ITO) pattern (6B) is formed on the gate pad (2B), so that the ITO pattern (6B) functions as a gate pad electrode and is directly contact over the gate insulating layer (3) (first insulating layer).

Claim 2, Shin discloses (col.1, lines 52 – 60) that the pixel electrode (6) is formed of transparent conductive material such as indium tin oxide (ITO).

Allowable Subject Matter

1. Claims 3-5 and 21-22 are allowed.
2. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record neither discloses nor teaches that a liquid crystal display device comprising various elements, more specifically, as the following:

the drain electrode has a through hole that exposes a portion of the first insulating layer, and the pixel electrode electrically contact an inner side surface of the drain electrode via the through hole [claim 3; as shown in Fig.6D];

the data pad contact hole passing through the doped amorphous silicon layer and passing through the amorphous silicon layer, and the data pad electrode electrically contact an inner side surface of the data pad via the data pad contact hole [claim 4; as shown in Fig.6D];

claim 21 is dependent on the claim 3; and claims 5 and 22 are dependent on the claim 4.

The closest references AAPA and US 5,825,449 (Shin) discloses a structure of a liquid crystal display device comprising a drain contact hole, a source pad contact hole (data pad contact hole) and a gate pad contact hole, but the prior art of record do not disclose the drain contact hole and the data pad (source pad) contact hole passing through the silicon layer (the pure amorphous silicon layer and the doped amorphous silicon layer), wherein the portions of the gate insulating layer are exposed and the pixel electrode or the data pad electrode contact the inner side surface of the drain electrode or the inner side surface of the data pad via the through holes as claimed in the claims.

Response to Arguments

3. Applicant's arguments with respect to claims 1-2 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 8:00 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mike Qi
March 31, 2004



DUNG T. NGUYEN
PRIMARY EXAMINER